IN THE SPECIFICATION

Please amend the paragraph beginning at page 1, line 22, as follows:

Some approaches have been examined to increase the memory capacity without carrying forward the miniaturization such as, for example, ~~to package~~ packaging plural memory chips ~~as being stacked~~, or ~~form~~ forming a three-dimensional memory chip with memory cell arrays stacked above a silicon substrate, and so on. However, conventionally proposed cell array stacking methods are such that planar cell arrays are simply stacked. In these cases, although N times capacity may be obtained by N layers stacking, cell accesses must be independently performed for the respective cell arrays. Therefore, it is not easy to access ~~to~~ plural cell arrays at ~~a~~ the same time.

Please amend the paragraph beginning at page 2, line 23, as follows:

In order to increase the capacity of such ~~the~~ a phase change memory, how to integrally form a cell array and a read/write circuit thereof becomes an important technical issue. Additionally, how to design the read/write circuit ~~capable~~ with the capability to perform high-speed data input/output ~~is~~ also becomes an important technical issue.

Please amend the paragraph beginning at page 6, line 4, as follows:

Referring to the drawings, embodiments of this invention will be described ~~bellow~~ below.

Please amend the paragraph beginning at page 7, line 1, as follows:

As previously stated, data is stored as the ~~significance of a~~ resistance value of the resistive element VR of each memory cell MC. For instance, in a non-select state, ~~let~~ all the word lines WL may be set at "L" level while ~~setting~~ all the bit lines BL may be set at "H"

level. One example is that "H" level is equal to 1.8V and "L" is 0V. In this ~~nonselect~~ non-select state, the diodes SD of all memory cells MC are in a reverse-bias state and thus are in an off-state; thus, no currents flow in the resistive elements VR. Considering the case of selecting a centrally located memory cell MC of the cell array of Fig. 1, which is surrounded by broken lines, ~~let~~ a selected word line WL is set at "H" while ~~setting~~ a selected bit line BL is set at "L." Whereby, at the selected cell, its diode SD becomes forward-biased allowing a current to flow therein.

Please amend the Abstract on page 46 as follows on the next page: